

COURSE OUTLINE

ENES-244

Digital Logic Design

3 Semester Hours

HOWARD COMMUNITY COLLEGE

Description

This course will introduce the basic principles and design procedures of digital systems at the gate and intermediate chip levels for electrical engineering students. The student will acquire knowledge of gates, flip-flops, registers, counters, Karnaugh maps, PAL devices, and synchronous sequential circuit design and analysis. Prerequisite: ENES-100 and MATH-133. (4 hours weekly)

Overall Course Objectives

Upon completion of this course, the student will be able to:

1. Convert between decimal, binary, octal, and hexadecimal number systems.
2. Do two-level logic minimization using Boolean algebra, Karnaugh maps, and the Quine-McCluskey tabular minimization method.
3. Describe the many types of logic gates.
4. Do binary addition and subtraction.
5. Incorporate medium scale integrated circuits, like decoders, encoders, multiplexers, etc., into circuit design.
6. Design and analyze clocked sequential circuits.
7. Use various types of latches and flip-flops to build binary memory.
8. Trace signals through various registers and counters.
9. Describe various types of memory parity and error correction algorithms.
10. Program PLA, PAL, SPLD devices.
11. Use algorithmic state machine notation.
12. Perform asynchronous sequential logic analysis.

Major Topics

- I. Binary Numbers, Arithmetic and Codes
- II. Boolean Algebra, Switching Algebra and Logic Gates
- III. Karnaugh Maps and simplification of Boolean functions
- IV. Combinational Design: Two-Level NAND/NOR implementation, Tabular Minimization
- V. Combinational Logic Design: add, subtract, convert code, check parity
- VI. MSI Components, design and use of encoders, decoders multiplexers, BCD adders, comparators
- VII. Latches and Flip-Flops
- VIII. Synchronous sequential circuit design and analysis
- IX. Registers, synchronous and asynchronous counters, and memory
- X. Control logic
- XI. Wired logic and characteristics of logic gate families
- XII. ROMs, PLDs, and PLAs

Course Requirements

Grading/exams: Grading procedures will be determined by the individual faculty member. Grades will be based on homework, tests and class participation.